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(54) Title: A LOW-COST METHOD OF PACKAGING MULTIPLE INTEGRATED CIRCUIT CHIPS IN A STANDARD SEMICONDUCTOR DEVICE PACKAGE INTENDED FOR A SINGLE CHIP

(57) **Abstract**

Provided is a method of packaging multiple integrated circuit chips in a standard semiconductor device package intended for a single chip. In one embodiment, a bottom surface of a larger first chip is attached to a die attach area of a standard semiconductor device package. A bottom surface of a smaller second chip is then attached to a top surface of the first chip. Bonding pads on a top surface of the second chip are electrically coupled to bonding pads on the top surface of the first chip. Bonding pads on the top surface of the first chip are then electrically coupled to bonding pads of the semiconductor device package. A heat spreader may also be positioned between the two chips in order to spread the heat energy generated by the second chip during operation over a wider surface area of the first chip. In a second embodiment, a decal including conductive traces is positioned between the two chips and used to route electrical signals from the bonding pads of one chip to the bonding pads of the other chip. In a third embodiment, bonding pads of a smaller second chip are electrically coupled to a first set of bonding pads on a top surface of a larger first chip using a flip-chip soldering technique.

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TITLE: A LOW-COST METHOD OF PACKAGING MULTIPLE INTEGRATED CIRCUIT CHIPS IN A STANDARD SEMICONDUCTOR DEVICE PACKAGE INTENDED FOR A SINGLE CHIP

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to semiconductor device manufacturing and more particularly to semiconductor device packaging.

2. Description of the Relevant Art

As digital integrated circuit manufacturing technologies mature, production yields of larger integrated circuits (i.e., chips) including greater numbers of devices with smaller feature sizes are increasing. The operating speeds of digital systems including such chips are now largely limited by the time it takes signals to travel through the signal lines (i.e., wires) which connect the chips to one another. In general, the longer the signal line between two chips, the longer it takes a signal to travel from one chip to the other along the signal line. The performance of a digital system may thus be increased by reducing the physical distances signals must travel between components (i.e., placing the chips closer together).

Integrated circuits are normally mounted within semiconductor device packages before being integrated into a system. Semiconductor device packages perform several basic functions. First, semiconductor device packages provide terminals to connect a chip to external circuitry. Such terminals include pins for insertion into holes in a socket, straight leads for insertion into holes in a printed circuit board (PCB), and bent leads which allow direct soldering of the leads to metal pads on the surface of a PCB. Semiconductor device packages also provide physical and environmental protection for a chip. In addition, semiconductor device packages carry heat generated by chips during operation away from the chips. Semiconductor device packages are selected based on performance requirements and cost considerations. Many standard types of semiconductor device packages intended for single chip packaging are available from a number of manufacturers at competitive prices. Device package costs typically increase with their ability to meet higher performance requirements.

Most modern high performance microprocessors benefit from having a relatively small, high-speed cache memory unit located in close proximity to a central processing unit (CPU). Accesses to such cache memory units are accomplished in much shorter periods of time than accesses to larger and slower main memory units, resulting in increases in overall system performances. Many microprocessors have cache memory units located on the same chip as the CPU. Others have cache memory units located on separate chips laterally mounted next to CPU chips within the same semiconductor device packages. Such

semiconductor device packages, carefully crafted to meet stringent performance requirements, are typically quite expensive.

The cost of designing and fabricating a custom semiconductor device package to contain both a CPU chip and a memory chip may represent a large portion of the cost of manufacturing the finished product. In order to reduce manufacturing costs, it would therefore be desirable to have a semiconductor device packaging technique which is based upon standard semiconductor device packages, intended for single chip packaging, and meets the requirements of two or more chips.

SUMMARY OF THE INVENTION

The problems outlined above are in large part solved by a low-cost method of packaging multiple integrated circuits in a standard semiconductor device package intended for a single chip. In one embodiment, a bottom surface of a larger first chip is attached to a die attach area of a standard semiconductor device package. A bottom surface of a smaller second chip is then attached to a top surface of the first chip. Bonding pads on a top surface of the second chip are electrically coupled to bonding pads on the top surface of the first chip. Bonding pads on the top surface of the first chip are then electrically coupled to bonding pads of the semiconductor device package. As a result, bonding pads of the second chip are electrically coupled to bonding pads of the first chip, and to bonding pads of the semiconductor device package. A heat spreader may also be positioned between the two chips in order to spread the heat energy generated by the second chip during operation over a wider surface area of the first chip.

In a second embodiment, a decal including conductive traces is used to route electrical signals from the bonding pads of one chip to the bonding pads of the other chip. The conductive traces of the decal interconnect a first and second set of bonding pads located on the top surface of the decal. As in the first embodiment, a bottom surface of a larger first chip is attached to a die attach area of a standard semiconductor device package. A bottom surface of the decal is then attached to a top surface of the first chip, and a bottom surface of a smaller second chip is attached to a top surface of the decal. Bonding pads on a top surface of the second chip are electrically coupled to the first set of bonding pads on the top surface of the decal. The second set of bonding pads on the top surface of the decal are then electrically coupled to bonding pads on the top surface of the first chip. Bonding pads on the top surface of the first chip are then electrically coupled to bonding pads of the semiconductor device package. Again, bonding pads of the second chip are electrically coupled to bonding pads of the first chip, and to bonding pads of the semiconductor device package.

In a third embodiment, bonding pads of a smaller second chip are electrically coupled to a first set of bonding pads on a top surface of a larger first chip using a flip-chip soldering technique. Bonding pads of the second chip are aligned with the first set of bonding pads of the first chip. The bonding pads of the second chip are then electrically coupled to the first set of bonding pads of the first chip using a flip-chip soldering technique. A bottom surface of the first chip is then attached to a die attach area of the semiconductor device package. A second set of bonding pads on the top surface of the first chip are electrically coupled to bonding pads of the semiconductor device package.

BRIEF DESCRIPTION OF THE DRAWINGS

Other objects and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

Fig. 1a is a perspective view of a standard pin grid array (PGA) package with a first and second integrated circuit chip mounted therein in accordance with a first embodiment of the present invention:

Fig. 1b is a partial cross-sectional view of the PGA package of Fig. 1a showing the two chips mounted within a chip cavity of the PGA package;

Fig. 2a is a top plan view of a chip cavity of a PGA package containing two chips mounted therein in accordance with a second embodiment of the present invention;

Fig. 2b is a partial cross-sectional view of the PGA package of Fig. 2a showing the two chips mounted within a chip cavity of the PGA package;

Fig. 3a is a top plan view of a chip cavity of a PGA package containing a first and second chip separated by a heat spreader;

Fig. 3b is a partial cross-sectional view of the PGA package of Fig. 3a showing the two chips separated by a heat spreader and mounted within the chip cavity of the PGA package;

Fig. 4a is a perspective view of a standard pin grid array (PGA) package with two integrated circuit chips bonded together using a flip-chip soldering technique and mounted therein in accordance with a third embodiment of the present invention;

Fig. 4b is a partial cross-sectional view of the PGA package of Fig. 4a showing the two chips bonded together and mounted within a chip cavity of the PGA package;

Fig. 5 is a flow chart of steps comprising the first embodiment of the present method;

Fig. 6 is a flow chart of steps included in the second embodiment of the present method: and

Fig. 7 is a flow chart of steps of the third embodiment of the present method.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE INVENTION

Figs. 1a and 1b will be used to describe a first embodiment of a method of mounting two integrated circuit chips within a standard semiconductor device package intended for a single chip. Suitable types of standard semiconductor device packages include pin grid array (PGA) packages, ball grid array (BGA) packages, and quad flatpacks. Fig. 1a is a perspective view of a standard pin grid array (PGA) package 10 with two integrated circuit chips 12 and 14 mounted therein. Fig. 1b is a partial cross-sectional view of PGA package 10 showing chips 12 and 14 mounted within a chip cavity 16 of PGA package 10. A bottom surface of a first chip 14 is attached to a substantially planar die attach area 18 of chip cavity 16 via a first bonding layer 20. Suitable attachment methods include well known eutectic and epoxy adhesive bonding. First bonding layer 20 also provides a thermally conductive path for heat energy to flow from first chip 14 to PGA package 10. When epoxy is used to attach the bottom surface of first chip 14 to PGA package 10, the thermal conductivity of first bonding layer 20 may be increased by the addition of metal particles to the epoxy adhesive material.

A bottom surface of a second chip 12 is then attached to a top surface of first chip 14 via a second bonding layer 22. A standard passivation layer (not shown) formed over the top surface of first chip 14 during fabrication protects first chip 14 from physical damage, moisture, and ionic species. Openings in the passivation layer allow access to bonding pads located on the top surface of first chip 14. Suitable methods to attach second chip 12 to first chip 14 include epoxy adhesive bonding. Second bonding layer 22 also provides a thermally conductive path for heat energy to flow from second chip 12 to first chip 14. The passivation layer protects first chip 14 and provides electrical isolation between first chip 14 and second chip 12.

In the embodiment of Figs. 1a and 1b, bonding pads (i.e., input/output terminals) of second chip 12 are directly connected to bonding pads of first chip 14, and bonding pads of first chip 14 are connected to bonding pads of PGA package 10. The bonding pads of PGA package 10 are connected to pins of PGA package 10. The pins of PGA package 10 thus function as terminals connecting both chips 12 and 14 to external circuitry. In Fig. 1b, bonding pad 24a of second chip 12 is electrically coupled to bonding pad 26a of first chip 14 by bond wire 28a. Bonding pad 26a of first chip 14 is electrically coupled to bonding pad 32a of PGA package 10 by bond wire 30a. Bonding pad 32a of PGA package 10 is electrically coupled to a pin 33a, shown in Fig. 1a, on an underside of PGA package 10. In a similar manner, bonding pad 24b of second chip 12 is electrically coupled to bonding pad 26b of first chip 14 by bond wire 28b. Bonding pad 26b of first chip 14 is electrically coupled to bonding pad 32b of PGA package 10 by bond wire 30b, and bonding pad 32b is

electrically coupled to a pin 33b on the underside of PGA package 10. Suitable electrical coupling methods for bonding pads include tape automated bonding (TAB) in addition to the wire bonding method described above. It is noted that one or more of the bonding pads of second chip 12 may be directly connected to bonding pads of PGA package 10.

Figs. 2a and 2b will be used to describe a second embodiment of the present invention. When bonding pads of two different chips mounted within a semiconductor device package do not align as to permit direct electrical connections without undesirable bonding wire crossovers, a decal including conductive traces may be used to route electrical signals from the bonding pads of one chip to the bonding pads of the other chip. Suitable types of standard semiconductor device packages include pin grid array (PGA) packages, ball grid array (BGA) packages, and quad flatpacks. Fig. 2a is a top plan view of a chip cavity 34 of a PGA package 36 containing a first chip 38 and a second chip 40. A bottom surface of first chip 38 is attached to a substantially planar die attach area 42 of chip cavity 34 via a first bonding layer 44 as described above. A bottom surface of second chip 40 is attached to a top surface of a decal 46, and a bottom surface of decal 46 is attached to a top surface of first chip 38. Suitable attachment methods include epoxy and polyimide adhesive bonding.

Decal 46 includes a first set of bonding pads 48 and a second set of bonding pads 50 interconnected by a network of conductive traces (i.e., wires) formed upon or within decal 46. Such conductive traces are typically formed by the masking and etching of a sheet of a conductive material. The first set of bonding pads 48 are electrically coupled to bonding pads of second chip 40, and the second set of bonding pads 50 are coupled to bonding pads of first chip 38. A conductive trace connects a bonding pad of first set of bonding pads 48 to one or more bonding pads of second set of bonding pads 50. In Fig. 2a, conductive trace 52 electrically connects bonding pad 54 of first set of bonding pads 48 to bonding pad 56 of second set of bonding pads 50. Decal 46 thus includes conductive traces which serve to route electrical signals from bonding pads of second chip 40 to bonding pads of first chip 38. The embodiment of Fig. 2a thus avoids bond wire crossover problems by using a high density network of conductive traces. Fig. 2b is a partial cross-sectional view of PGA package 36 showing chips 38 and 40 mounted within a chip cavity 34 of PGA package 36. In Fig. 2b, bonding pad 58a of second chip 40 is electrically coupled to bonding pad 60a of decal 46 by bond wire 62a. Bonding pad 64a of decal 46 is electrically coupled to bonding pad 66a of first chip 38 by bond wire 68a. Bonding pad 66a of first chip 38 is electrically coupled to bonding pad 70a of PGA package 36 by bond wire 72a, and bonding pad 70a is electrically coupled to a pin on the underside of PGA package 36. Should a conductive trace electrically couple bonding pads 60a and 64a of decal 46, bonding pads of both chips 38 and 40 would be electrically coupled to the same pin of PGA package 36. In a similar manner, bonding pad 58b of second chip 40 is electrically coupled to bonding pad 60b of decal 46 by bond wire 62b. Bonding pad 64b of decal 46 is electrically coupled to bonding pad 66b of first chip 38 by bond wire 68b. Bonding pad 66b of first chip 38 is electrically coupled to bonding pad 70b of PGA package 36 by bond wire 72b, and bonding pad 70b is electrically coupled to a pin on the underside of PGA package 36. A TAB technique may also be used to electrically couple bonding pads. It is noted that one or more of the bonding pads of second chip 40 may be directly connected to bonding pads of PGA package 36.

Decal 46 may be a single patterned conductive metal layer bonded between two layers of a dielectric material. Holes formed in an upper dielectric layer allow access to the first and second sets of bonding pads. Suitable conductive metals include copper and aluminum. Suitable dielectric materials include polyimide and polyester films. Decal 46 may also have multiple patterned metal layers, wherein each patterned metal layer is separated from an adjacent patterned metal layer by a layer of a dielectric material. In this case, traces of two different conductive layers may be electrically connected in holes formed in the dielectric layers separating the two conductive layers. Decal 46 may be formed using well known TAB tape manufacturing methods.

Figs. 3a and 3b will be used to describe a variation of the first embodiment wherein a heat spreader (i.e., a thermally conductive plate) is positioned between two chips mounted within a standard semiconductor device package. The heat spreader spreads the heat energy generated by the second chip during operation over a wider surface area of the first chip. Fig. 3a is a top plan view of a chip cavity 74 of a PGA package 76 containing a first chip 78 and a second chip 80. Fig. 3b is a partial cross-sectional view of PGA package 76 showing chips 78 and 80 mounted within a chip cavity 74 of PGA package 76. A bottom surface of second chip 80 is attached to a top surface of a heat spreader 82, and a bottom surface of heat spreader 82 is attached to a top surface of first chip 78. Suitable attachment methods include epoxy and polyimide adhesive bonding.

Heat spreader 82 provides a thermally conductive path for heat energy to flow from second chip 80 to first chip 78 during operation. A standard passivation layer (not shown) formed over first chip 78 during fabrication protects first chip 78 and provides electrical isolation between first chip 14 and heat spreader 82. Heat spreader 82 has two major surfaces, each with a lateral surface area greater than second chip 80 but less than first chip 78. Heat spreader 82 spreads heat energy generated by second chip 80 during operation over a wider area of the top surface of first chip 78, thus reducing the amount of heat energy transferred to first chip 78 per unit of surface area. Heat spreader 82 may thus find utility when second chip 80 dissipates an appreciable amount of electrical energy during operation. Suitable materials for heat spreader 82 include aluminum, silicon, and aluminum nitride.

Figs. 4a and 4b will be used to describe a third embodiment of the present invention in which a smaller second chip is attached to a larger first chip using flip-chip (controlled collapse) bonding, and the bonded chips are mounted within a standard semiconductor device package intended for a single chip. In this embodiment both chips are designed and fabricated such that bonding pads of the second chip align with a first set of bonding pads of the first chip. The bonding pads of the second chip and the first set of bonding pads of the first chip are prepared such that raised metallic bumps are formed on the bonding pads. The raised metallic bumps are typically made of solder. The bonding pads of the second chip and the first set of bonding pads of the first chip are then bonded together using a reflow soldering technique. Suitable types of standard semiconductor device packages include pin grid array (PGA) packages, ball grid array (BGA) packages, and quad flatpacks. Fig. 4a is a perspective view of a standard pin grid array (PGA) package 84 with two integrated circuit chips 86 and 88 bonded together using a flip-chip bonding method and mounted therein.

Fig. 4b is a partial cross-sectional view of PGA package 84 showing chips 86 and 88 bonded together and mounted within a chip cavity 90 of PGA package 84. Bonding pads 94a-b and 95a-b of first chip 88 are

included in a first set of bonding pads of first chip 88. During a flip-chip bonding process, bonding pad 92a of second chip 86 is joined to bonding pad 94a of first chip 88 by solder ball 96a. Similarly, bonding pad 92b of second chip 86 is joined to bonding pad 94b of first chip 88 by solder ball 96b. Bonding pads 93a and 93b of second chip 86 are joined to bonding pads 95a and 95b of first chip 88, respectively, in a similar manner. Accordingly, second chip 86 is bonded to first chip 88 in an inverted position. After the chips have been bonded together, a bottom surface of first chip 88 is attached to a substantially planar die attach area 98 of chip cavity 90 via a bonding layer 100 as described above. Bonding layer 100 also provides a thermally conductive path for heat energy to flow from first chip 88 to PGA package 84.

Bonding pads 102a and 102b of first chip 88 are included in a second set of bonding pads of first chip 88. Bonding pads in the second set of bonding pads of first chip 88 may be directly connected to bonding pads in the first set of bonding pads of first chip 88. For example, electrical conductor 103 may directly connect bonding pad 94b and bonding pad 102b as shown in Fig. 4b. Bonding pads of the second set of bonding pads of first chip 88 are connected to bonding pads of PGA package 84. The bonding pads of PGA package 84 are connected to pins of PGA package 84, which function as terminals connecting both chips 86 and 88 to external circuitry. In Fig. 4b, bonding pad 102a of first chip 88 is electrically coupled to bonding pad 104a of PGA package 84 by bond wire 106a. Bonding pad 104a of PGA package 84 is electrically coupled to a pin 107a on an underside of PGA package 84. In a similar manner, bonding pad 102b of first chip 88 is electrically coupled to bonding pad 104b of PGA package 84 by bond wire 106b, and bonding pad 104b is electrically coupled to a pin 107b on the underside of PGA package 84. Alternately, a TAB technique may be used to electrically couple the second set of bonding pads of first chip 88 to bonding pads of PGA package 84.

Although Figs. 1a-4b show only two integrated circuit chips, it is noted that the above method may be used to mount two or more chips within a standard semiconductor device package intended for a single chip.

Fig. 5 is a flow chart of steps comprising the first embodiment of the present method of mounting a larger first integrated circuit chip and a smaller second integrated circuit chip within a standard semiconductor device package intended for a single chip. During a step 108, a bottom surface of the first chip is attached to a die attach area of a standard semiconductor device package as described above. A bottom surface of the second chip may then be attached to a top surface of the first chip during a step 110. Alternately, a heat spreader may be positioned between the two chips. A bottom surface of the heat spreader may be attached to the top surface of the first chip during a step 112, and a bottom surface of the second chip may be attached to a top surface of the heat spreader during a set 114. During a step 116, bonding pads on a top surface of the second chip are electrically coupled to bonding pads on the top surface of the first chip as described above. Bonding pads on the top surface of the first chip are then electrically coupled to bonding pads of the semiconductor device package during a step 118.

Fig. 6 is a flow chart of steps included in the second embodiment of the present method of mounting a larger first chip and a smaller second chip within a standard semiconductor device package intended for a single chip. In this case, a decal including conductive traces is used to route electrical signals from the

bonding pads of one chip to the bonding pads of the other chip. During a step 120, a bottom surface of the first chip is attached to a die attach area of a standard semiconductor device package as described above. A bottom surface of the decal is then attached to a top surface of the first chip during a step 122. During a step 124, a bottom surface of the second chip is attached to a top surface of the decal. Bonding pads on a top surface of the second chip are electrically coupled to a first set of bonding pads accessible from the top surface of the decal as described above during a step 126. During a step 128, a second set of bonding pads accessible from the top surface of the decal are electrically coupled to bonding pads on the top surface of the first chip. Bonding pads on the top surface of the first chip are then electrically coupled to bonding pads of the semiconductor device package as described above during a step 130.

Fig. 7 is a flow chart of steps of the third embodiment of the present method of mounting a larger first chip and a smaller second chip within a standard semiconductor device package intended for a single chip. In this method, bonding pads of the second chip are electrically coupled to a first set of bonding pads on a top surface of a larger first chip using a flip-chip soldering technique. Bonding pads of the second chip are aligned with the first set of bonding pads on a top surface of the first chip during a step 132. During a step 134, the bonding pads of the second chip are electrically coupled to the first set of bonding pads of the first chip using a flip-chip technique described above. A bottom surface of the first chip is then attached to a die attach area of the semiconductor device package as described above during a step 136. During a step 138, a second set of bonding pads on the top surface of the first chip are electrically coupled to bonding pads of the semiconductor device package as described above.

It will be appreciated to those skilled in the art having the benefit of this disclosure that this invention is believed to be a low-cost method of packaging multiple integrated circuits in a standard semiconductor device package intended for a single chip. Furthermore, it is also to be understood that the form of the invention shown and described is to be taken as exemplary, presently preferred embodiments. Various modifications and changes may be made without departing from the spirit and scope of the invention as set forth in the claims. It is intended that the following claims be interpreted to embrace all such modifications and changes.

WHAT IS CLAIMED IS:

1. A method of packaging a larger first integrated circuit chip and a smaller second integrated circuit chip within a semiconductor device package intended for a single chip, comprising:

attaching a bottom surface of the first chip to a die attach area of the semiconductor device package;

attaching a bottom surface of the second chip to a top surface of the first chip;

electrically coupling a bonding pad on a top surface of the second chip to a bonding pad on the top surface of the first chip; and

electrically coupling the bonding pad on the top surface of the first chip to a bonding pad of the semiconductor device package.

2. The method as recited in claim 1, wherein the bottom surface of the first chip is attached to the die attach area of the semiconductor device package by eutectic bonding.

3. The method as recited in claim 1, wherein the bottom surface of the first chip is attached to the die attach area of the semiconductor device package by epoxy adhesive bonding.

4. The method as recited in claim 3, wherein the epoxy used to attach the bottom surface of the first chip to the

die attach area of the semiconductor device package contains metal particles to provide improved thermal conductivity.

5. The method as recited in claim 1, wherein the bottom surface of the second chip is attached to the top surface of the first chip by epoxy adhesive bonding.

6. The method as recited in claim 5, wherein the epoxy used to attach the bottom surface of the second chip to the top surface of the first chip contains metal particles to provide improved thermal conductivity.

7. The method as recited in claim 1, wherein the bonding pad of the second chip is electrically coupled to the bonding pad of the first chip by wire bonding.

8. The method as recited in claim 7, wherein the bonding pad of the second chip is electrically coupled to the bonding pad of the first chip by tape automated bonding.

9. The method as recited in claim 1, wherein the bonding pad of the first chip is electrically coupled to the bonding pad of the semiconductor device package by wire bonding.

10. The method as recited in claim 1, wherein the bonding pad of the first chip is electrically coupled to the bonding pad of the semiconductor device package by tape automated bonding.

11. The method as recited in claim 1, further comprising inserting a heat spreader between the first and second chips.

12. The method as recited in claim 11, wherein the heat spreader comprises aluminum.

13. A method of packaging a larger first integrated circuit chip and a smaller second integrated circuit chip within a semiconductor device package intended for a single chip, comprising:

attaching a bottom surface of the first chip to a die attach area of the semiconductor device package;

attaching a bottom surface of a decal to a top surface of the first chip;

attaching a bottom surface of the second chip to a top surface of the decal;

electrically coupling a bonding pad on a top surface of the second chip to a first bonding pad accessible from the top surface of the decal;

electrically coupling a second bonding pad accessible from the top surface of the decal to a bonding pad on the top surface of the first chip; and

electrically coupling the bonding pad on the top surface of the first chip to a bonding pad of the semiconductor device package.

14. The method as recited in claim 13, wherein the bottom surface of the first chip is attached to the die attach area

of the semiconductor device package by eutectic bonding.

15. The method as recited in claim 13, wherein the bottom surface of the first chip is attached to the die attach area of the semiconductor device package by epoxy adhesive bonding.

16. The method as recited in claim 15, wherein the epoxy used to attach the bottom surface of the first chip to the die attach area of the semiconductor device package contains metal particles to provide improved thermal conductivity.

17. The method as recited in claim 13, wherein the decal comprises a single patterned conductive metal layer bonded between two layers of a dielectric material.

18. The method as recited in claim 17, wherein the conductive metal layer comprises copper.

19. The method as recited in claim 17, wherein the dielectric material comprises polyimide.

20. The method as recited in claim 13, wherein the decal comprises a plurality of patterned metal layers, and wherein each of the plurality of patterned metal layers is separated from an adjacent patterned metal layer by a layer of a dielectric material.

21. The method as recited in claim 13, wherein the bottom surface of the decal is attached to the top surface of the first chip by epoxy adhesive bonding.

22. The method as recited in claim 13, wherein the bottom surface of the decal is attached to the top surface of the first chip by polyimide adhesive bonding.

23. The method as recited in claim 13, wherein the bottom surface of the second chip is attached to the top surface of the decal by epoxy adhesive bonding.

24. The method as recited in claim 13, wherein the bottom surface of the second chip is attached to the top surface of the decal by polyimide adhesive bonding.

25. The method as recited in claim 13, wherein the bonding pad on the top surface of the second chip is electrically coupled to the first bonding pad of the decal by wire bonding.

26. The method as recited in claim 13, wherein the bonding pad on the top surface of the second chip is electrically coupled to the first bonding pad of the decal by tape automated bonding.

27. A method of packaging a larger first integrated circuit chip and a smaller second integrated circuit chip within a semiconductor device package intended for a single chip, comprising:

aligning, in direct contact with one another, a set of bonding pads of the second chip with a first set of bonding pads on a top surface of the first chip;

electrically coupling the set of bonding pads of the second chip with the first set of bonding pads of the first chip;

attaching a bottom surface of the first chip to a die attach area of the semiconductor device package; and

electrically coupling a second set of bonding pads on the top surface of the first chip to a set of bonding pads of the semiconductor device package.

28. The method as recited in claim 27, wherein the set of bonding pads of the second chip are electrically coupled to the first set of bonding pads of the first chip using flip-chip soldering.

29. The method as recited in claim 27, wherein the bottom surface of the first chip is attached to the die attach area of the semiconductor device package by eutectic bonding.

30. The method as recited in claim 13, wherein the bottom surface of the first chip is attached to the die attach area of the semiconductor device package by epoxy adhesive bonding.

31. The method as recited in claim 30, wherein the epoxy used to attach the bottom surface of the first chip to the die attach area of the semiconductor device package contains metal particles to provide improved thermal conductivity.

32. The method as recited in claim 27, wherein the second

set of bonding pads on the top surface of the first chip are electrically coupled to the set of bonding pads of the semiconductor device package by wire bonding.

33. The method as recited in claim 27, wherein the second set of bonding pads on the top surface of the first chip are electrically coupled to the set of bonding pads of the semiconductor device package by tape automated bonding.

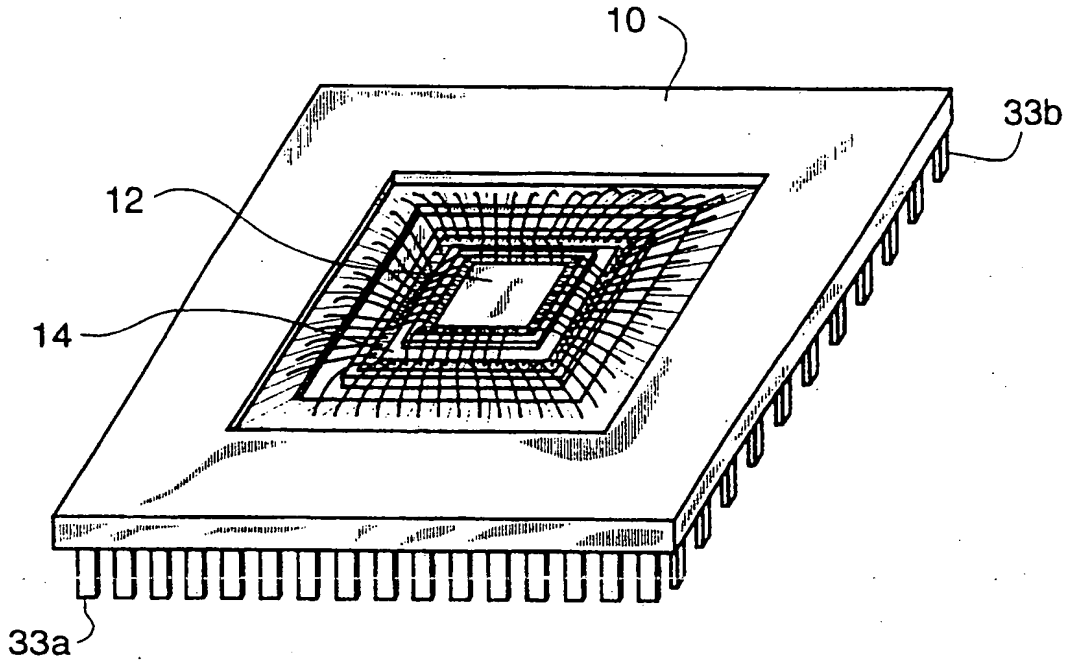

FIG. 1a

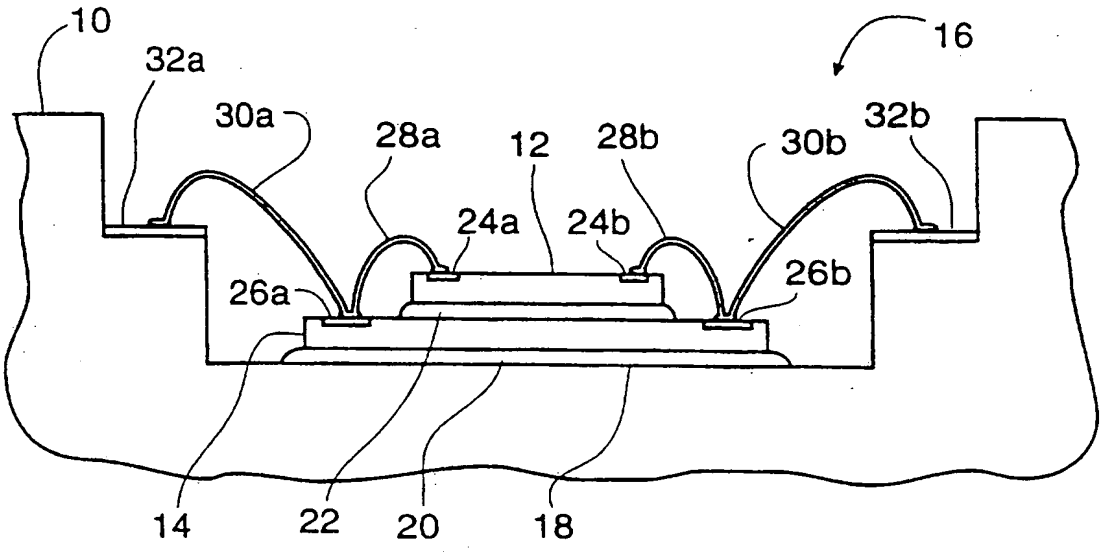

FIG. 1b

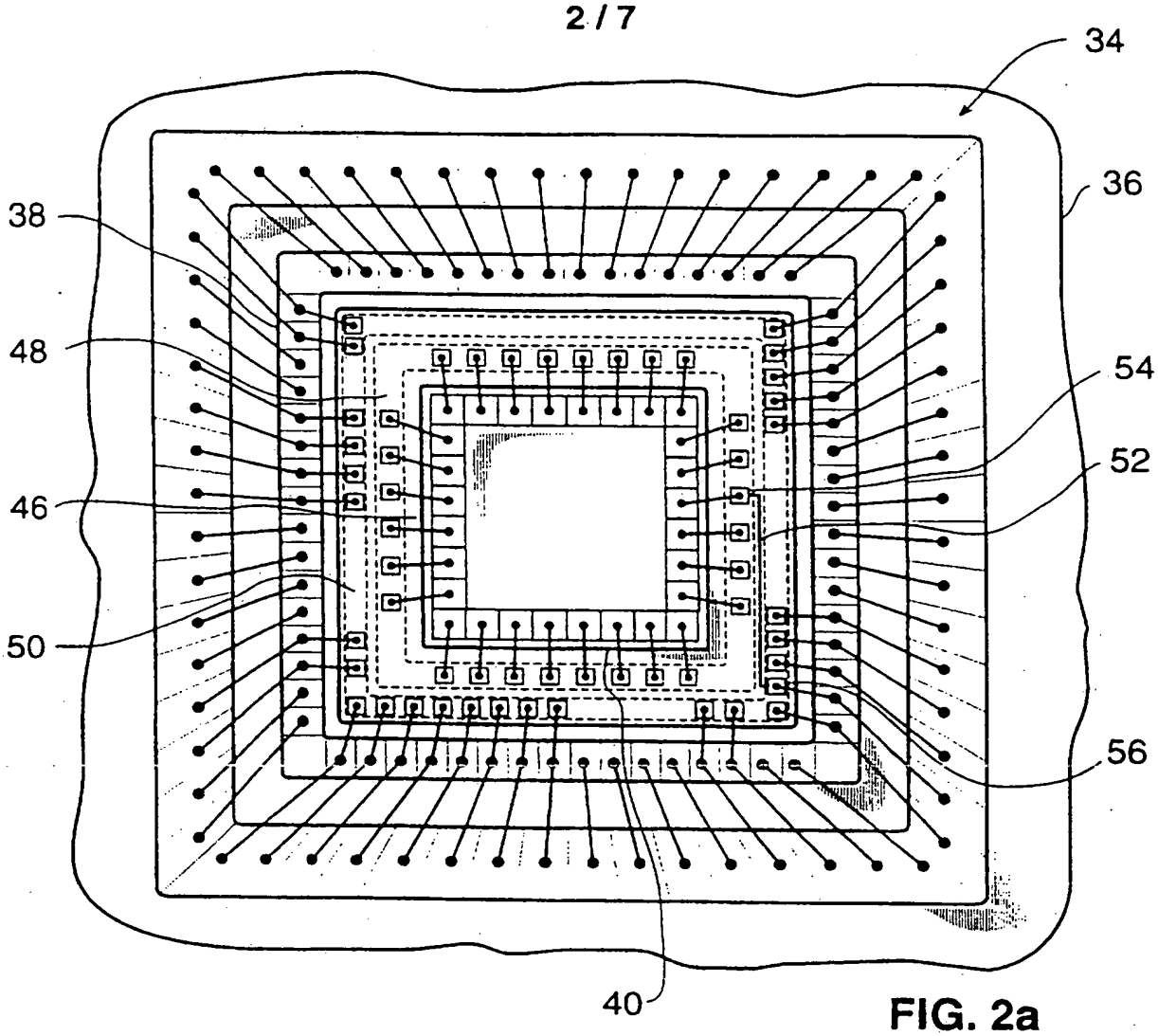

FIG. 2a

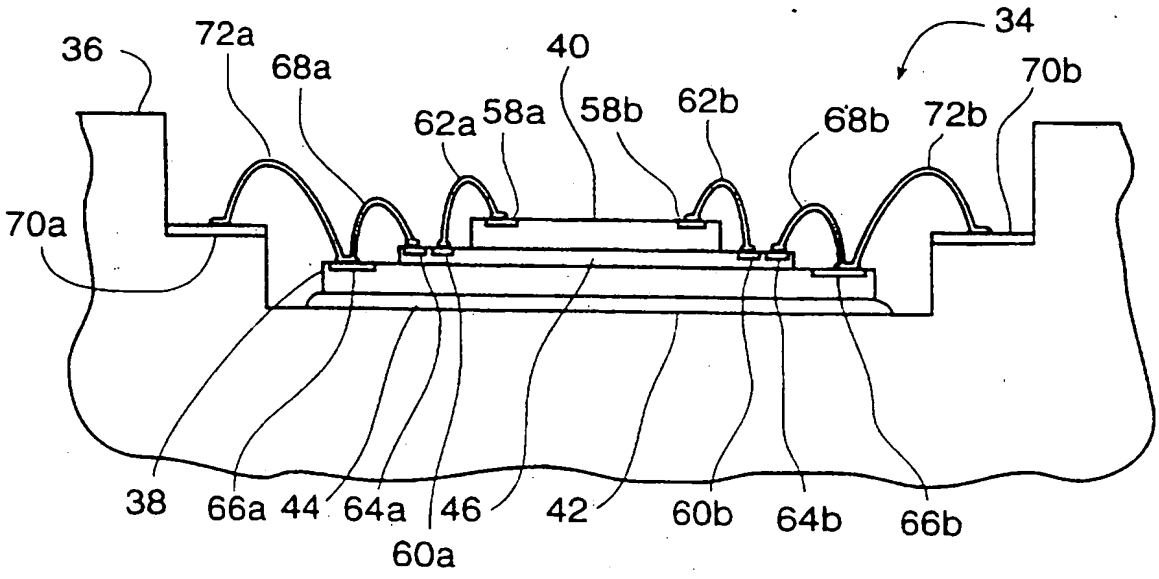

FIG. 2b

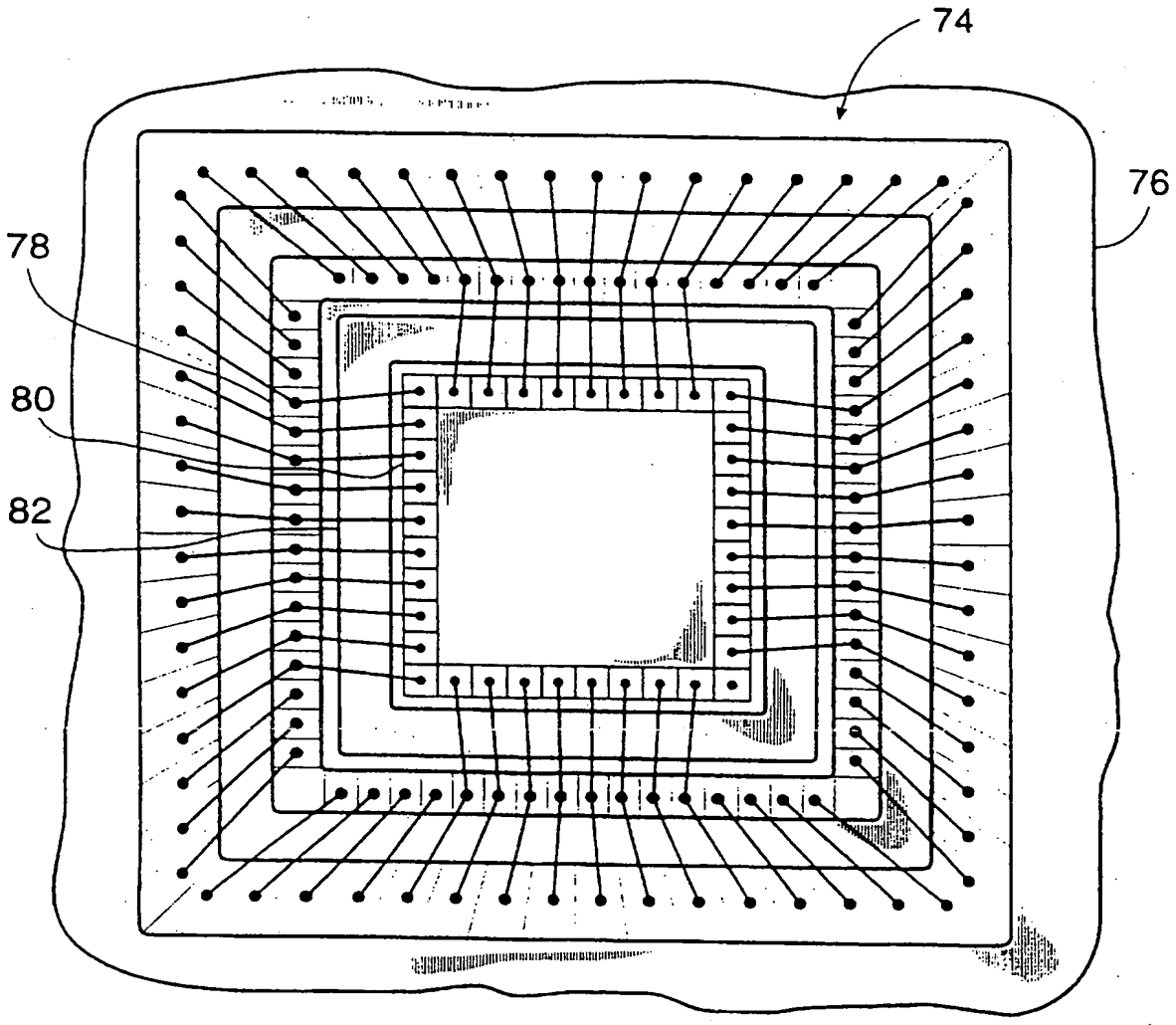

FIG. 3a

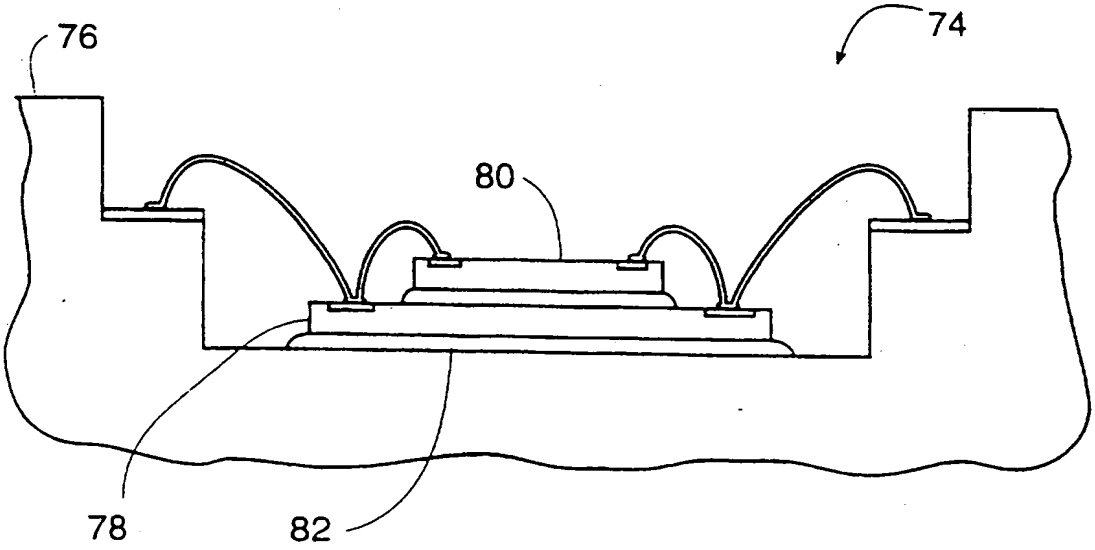

FIG. 3b

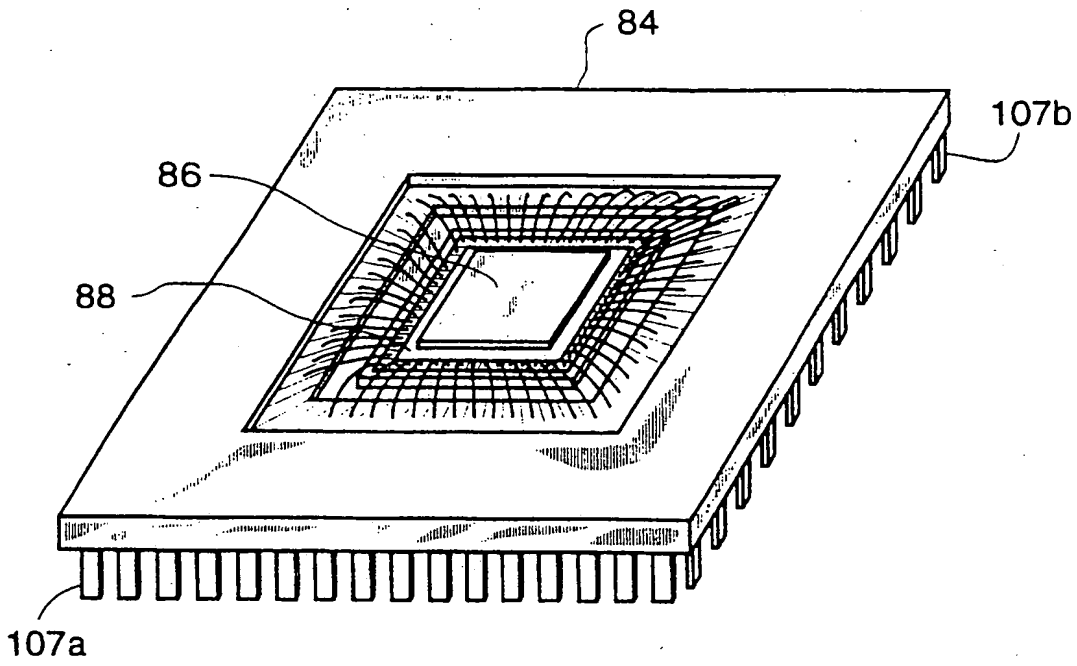

FIG. 4a

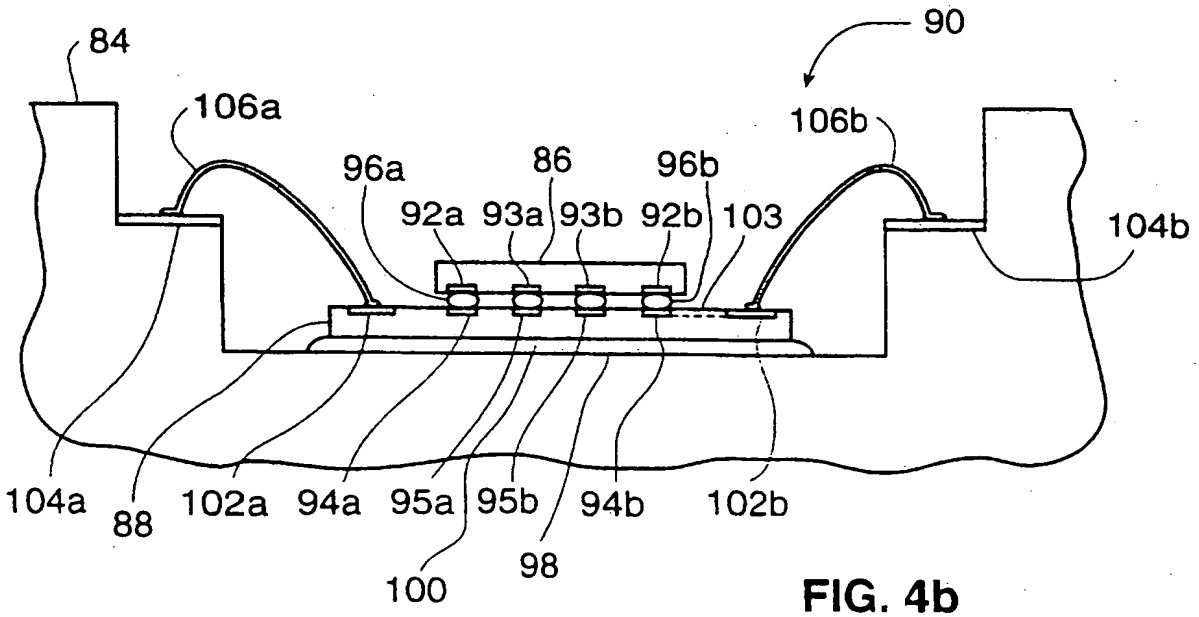

FIG. 4b

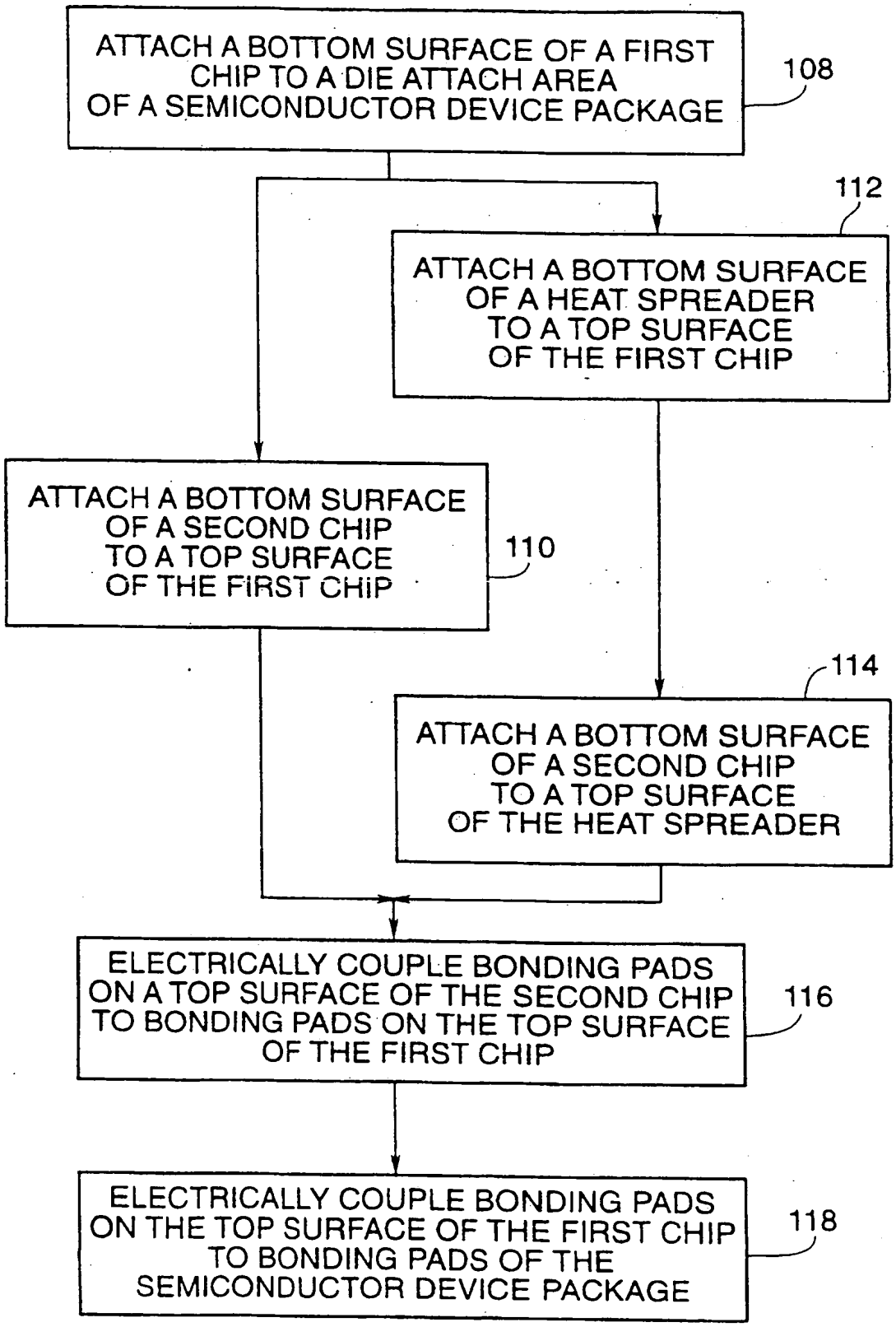

FIG. 5

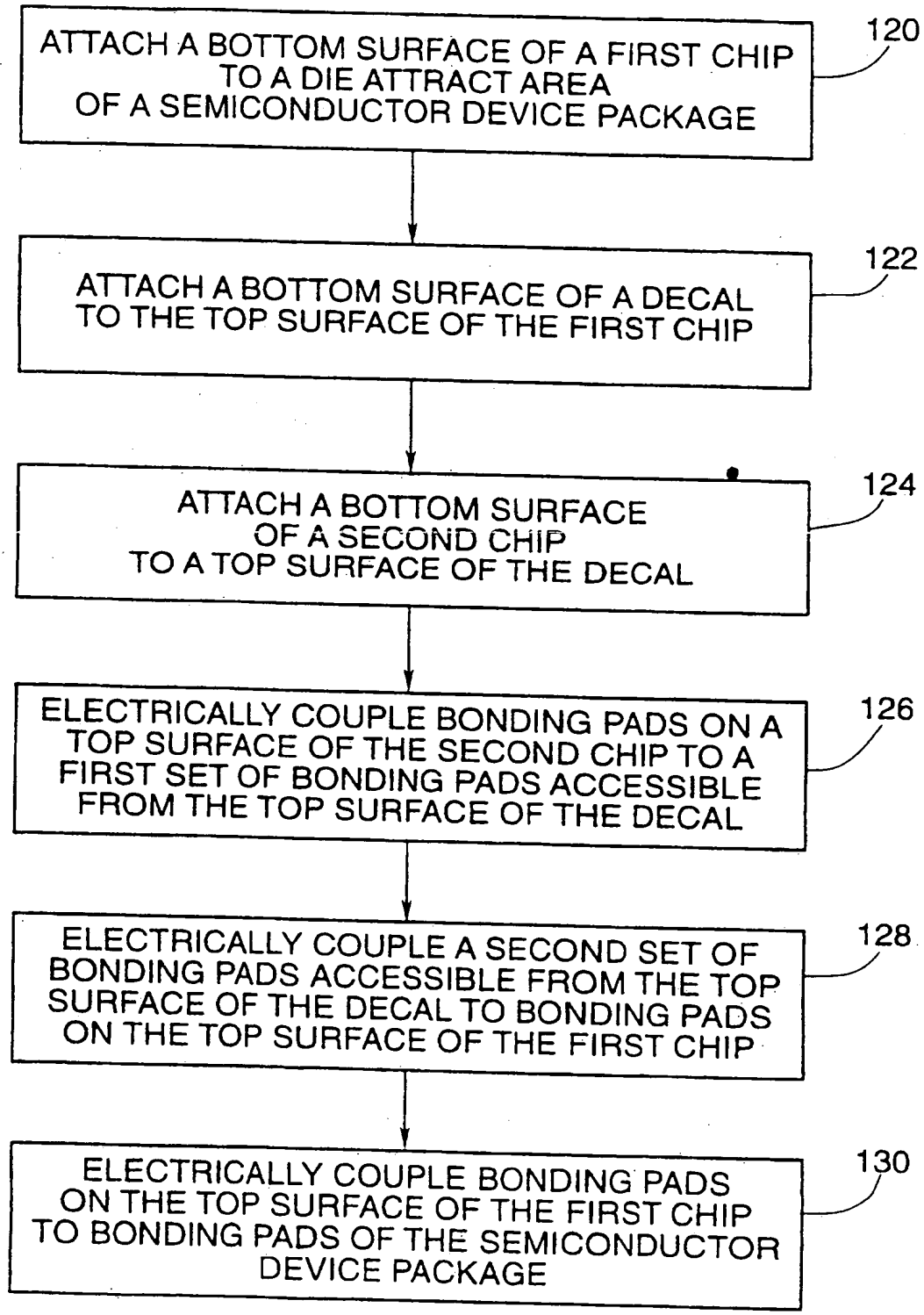

FIG. 6

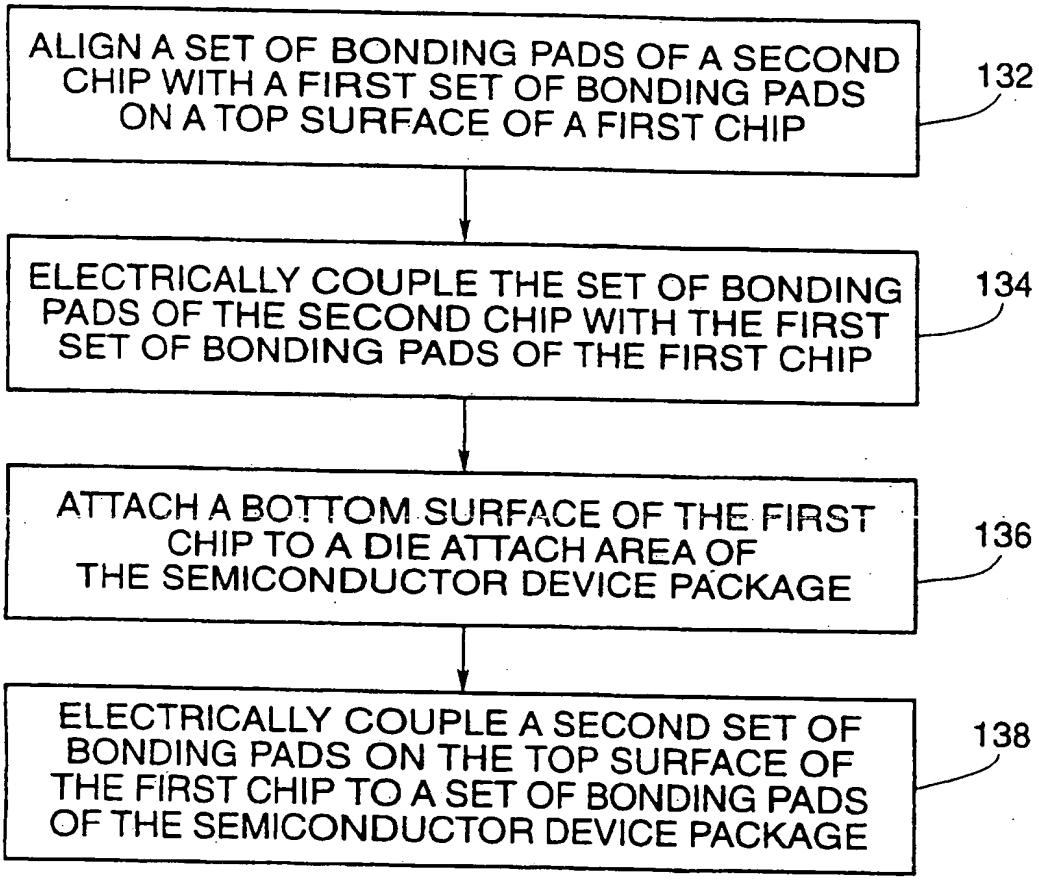

FIG. 7

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(72) Inventor: HERRELL, Dennis. J.; 6605 Serena Cove, Austin, TX 78730 (US).

(74) Agent: MILLER, Louise, K.; Advanced Micro Devices, Inc., 5204 East Ben White Boulevard, M/S 562, Austin, TX 78741 (US).

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(57) Abstract

Provided is a method of packaging multiple integrated circuit chips in a standard semiconductor device package intended for a single chip. In one embodiment, a bottom surface of a larger first chip (14) is attached to a die attach area (18) of a standard semiconductor device package. A bottom surface of a smaller second chip (12) is then attached to a top surface of the first chip. Bonding pads (24a, 24b) on a top surface of the second chip are electrically coupled (28a, 28b) to bonding pads (26a, 26b) on the top surface of the first chip. Bonding pads on the top surface of the first chip are then electrically coupled to bonding pads (32a, 32b) of the semiconductor device package. A heat spreader (82) may also be positioned between the two chips in order to spread the heat energy generated by the second chip during operation over a wider surface area of the first chip. In a second embodiment, a decal (46) including conductive traces is positioned between the two chips and used to route electrical signals from the bonding pads of one chip to the bonding pads of the other chip. In a third embodiment, bonding pads of a smaller second chip are electrically coupled to a first set of bonding pads on a top surface of a larger first chip using a flip-chip soldering technique.

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INTERNATIONAL SEARCH REPORT

International Application No
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According to International Patent Classification (IPC) or to both national classification and IPC

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y	see column 9, line 19 - column 10, line 32; figures 3-7	11,22,24

Y	PATENT ABSTRACTS OF JAPAN vol. 012, no. 135 (E-604), 23 April 1988 & JP 62 261166 A (MATSUSHITA ELECTRONICS CORP), 13 November 1987, see abstract	11

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1

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Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	**Authorized officer** Le Minh, I

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A	see column 6, line 13 - column 7, line 40; figures 4A-C,5,6A-C	13,25,26
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A	see the whole document	13
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